Development of a non-equilibrium electronic structure calculation method based on local constrained density functional theory: Applications to vertically-stacked 2D heterostructures

Han Seul Kim and Yong-Hoon Kim*

Graduate School of EEWS, KAIST, 291 Daehak-ro, Yuseong-gu, Daejeon 305-701, Republic of Korea *y.h.kim@kaist.ac.kr

Abstract

We report on the development of a novel first-principles electronic structure calculation method for the junction systems subjected to non-equilibrium conditions. Within the scheme, non-equilibrium situations induced by external bias voltages are described within the local constrained density functional theory formalism. We will discuss our solutions to the several technical difficulties in describing complicated nanointerfaces placed under bias voltages. As application examples, we consider vertically-stacked van der waals heterostructure based on two-dimensional layered materials. By explicitly extracting the changes in energy level alignment and charge transfer characteristics in response to the source-drain and gate biases, we provide atomistic guidelines for the design of several novel nano-devices.